UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,673	12/08/2000	Yoshitami Sakaguchi	JP919990237US1(13998)	2711

7590 08/03/2005

Richard L. Catania, Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, NY 11530

EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/733,673	SAKAGUCHI ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,13,15 and 16* is/are allowed.

6)☒ Claim(s) *1,3-7,9,10,12 and 14* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US Patent No. 6,211,849 B1) in view of Arsenault et al. (US Patent No. 6, 658,661 B1), Hamai (US Patent No. 5,148,263) and Richards et al. (US Patent No. 5,513,115).

As to claim 1, Sasaki et al. teaches a liquid crystal display device with: a crystal cell forms an image display area on substrate (See Fig.2, item 22, in description See from Col. 2, Line 50 to Col.4, Line 3); a driver for applying a voltage to liquid crystal cell based on an input video signal, wherein driver includes a plurality of driver ICs that mounted on substrate (See Figs. 2-3, items 1-3,10,23 in description See Col. 4, Lines) and a plurality of signal lines, each of the signal lines passing through each of the driver ICs in series, wherein driver ICs are cascade-connected in series using signal lines (See Fig. 3, items 1-3,10, in description See Col. 4, Lines 34-43), wherein plurality of driver IC are cascade-connected to a power feed line (See Fig. 3, items 1, VDD, Col. 4, Lines 28-34).

Sasaki et al. does not show the driver receives a digital packet signal including input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC.

Arsenault et al. teaches to generate a digital packet information including input video signal (See Fig. 2, items 58, 60, 72, 84, in description See Col. 6, Lines 1-10) an how to filter incoming data by bit mask (See Fig. 5, item 140, in description See Col. 7, Lines 23-34 and Col. 2, Lines 39-40).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. controller using Arsenault et al. approach to generate a digital packet signal including input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC since digital packets and masking has been well known and inexpensive.

Sasaki et al. and Arsenault et al. do not show connections to a power feed line via a metal layer inside of each driver ICs.

Hamai teaches outside power pad being connected to inside metal layers (See Fig. 1, items 2, 6, Col. 1, Lines 17-35).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Hamai teaching into Sasaki et al. and Arsenault et al. system in order to reduce area of power supply lines inside of the chip (See Col. 1, Lines 60-65 in the Hamai reference).

Arsenault et al., Sasaki et al. and Hamai do not disclose transmitting a wait bit block to a succeeding driver IC in series.

Richards et al. teaches disclose transmitting a wait block (See Fig. 10, item 130, from Col. 20, Line 54 to Col. 21, Line 18).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Richards et al. teaching into Sasaki et al., Hamai and Arsenault et al. system in order improved control system (See Col. 4, Lines 6-9 in the Richards et al. reference).

As to claim 4, Sasaki et al. teaches a liquid crystal display device with: a crystal cell forms an image display area on substrate (See Fig.2, item 22, in description See from Col. 2, Line 50 to Col.4, Line 3); a driver for distributing an input video signal to a plurality of driver ICs chain-connected in series using a plurality of signal lines (See Figs. 2-3, items 1-3,10,23 in description See Col. 4, Lines), each of the signal lines passing through each of the driver ICs in series, and for applying a voltage to LCD cell by employing driver ICs, wherein driver distributes video signal to plurality of driver ICs (See Fig. 3, items 1-3,10, in description See Col. 4, Lines 34-43).

Sasaki et al. does not show the driver receives a digital packet signal including input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC.

Arsenault et al. teaches to generate a digital packet information including input video signal (See Fig. 2, items 58, 60, 72, 84, in description See Col. 6, Lines 1-10) an how to filter incoming data by bit mask (See Fig. 5, item 140, in description See Col. 7, Lines 23-34 and Col. 2, Lines 39-40).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. controller using Arsenault et al. approach to generate a digital packet signal including input video signal and each driver IC includes a controller for generating a mask

signal to mask video data output from the driver IC since digital packets and masking has been well known and inexpensive.

Arsenault et al., Sasaki et al. do not disclose transmitting a wait bit block to a succeeding driver IC in series.

Richards et al. teaches disclose transmitting a wait block (See Fig. 10, item 130, from Col. 20, Line 54 to Col. 21, Line 18).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Richards et al. teaching into Sasaki et al., Hamai and Arsenault et al. system in order improved control system (See Col. 4, Lines 6-9 in the Richards et al. reference).

As to claim 6, Sasaki et al. teaches a liquid crystal display device comprising: a liquid crystal cell forms an image display area on substrate (See Fig.2, item 22, in description See from Col. 2, Line 50 to Col.4, Line 3); a driver for distributing an input video signal to a plurality of driver ICs that are cascade-connected (See Figs. 2-3, items 1-3,10,23 in description See Col. 4, Lines 27-45), and for applying a voltage to LC cell by employing driver ICs (see Fig. 3, items 1-3,10, in description See Col. 4, Lines 34-43 and Col. 3, Lines 1-10), wherein plurality of driver ICs of driver are cascade connected in series by a video transmission line provided on substrate, video transmission line passing through each of driver IC's in series and controlled by serial control that are transmitted along video transmission line (See Figs, 3-4, items 1-2, 10, DATA, CNT, in Description See Col. 4, Line 28-67), wherein plurality of driver IC are cascade-connected to a power feed line (See Fig. 3, items 1, VDD, Col. 4, Lines 28-34).

Sasaki et al. does not show the driver controlled by serial data line and receives a digital packet signal including input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC.

Arsenault et al. teaches to generate a digital packet information including input video signal (See Fig. 2, items 58, 60, 72, 84, in description See Col. 6, Lines 1-10) an how to filter incoming data by bit mask (See Fig. 5, item 140, in description See Col. 7, Lines 23-34 and Col. 2, Lines 39-40).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. controller using Arsenault et al. approach to the driver controlled by serial data line and generate a digital packet signal including input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC since digital packets and masking has been well known and inexpensive.

Sasaki et al. and Arsenault et al. do not show connections to a clock and power line via a metal layer inside of each driver ICs.

Hamai teaches outside power pad being connected to inside metal layers (See Fig. 1, items 2, 6, Col. 1, Lines 17-35).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Hamai teaching into Sasaki et al. and Arsenault et al. system including a clock line in order to reduce area of power supply lines inside of the chip (See Col. 1, Lines 60-65 in the Hamai reference).

Arsenault et al., Sasaki et al. and Hamai do not disclose transmitting a wait bit block to a succeeding driver IC in series.

Richards et al. teaches disclose transmitting a wait block (See Fig. 10, item 130, from Col. 20, Line 54 to Col. 21, Line 18).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Richards et al. teaching into Sasaki et al., Hamai and Arsenault et al. system in order improved control system (See Col. 4, Lines 6-9 in the Richards et al. reference).

As to claim 7, Sasaki et al. does not teach about a second signal line for which the polarity of first signal line has been inverted. As notoriously well known in the art a line with polarity of first signal line has been inverted could be easily implemented.

It would have been obvious to the one ordinary skill in the art in the time of invention to add a second signal line for which the polarity of first signal line has been inverted to Sasaki et al., and Arsenault et al. apparatus in order to reduce size and increase reliability of the LCD display device.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al., Arsenault et al., Hamai and Richards et al. as aforementioned in claim 4 in view of Shimizu (US Patent No. 5,801,674).

As to claim 5, Sasaki et al., Arsenault et al., Hamai and Richards et al. do not teach downstream driver applies a voltage to LC cell in accordance with input video signal after receiving masking signal from upstream driver IC.

Shimizu teaches about downstream driver applies a voltage to LC cell in accordance with input video signal after receiving masking signal from upstream driver IC (See Fig. 1, items 3-6, ENABLE1-ENABLE6, in description See Col. 3, Lines 67-68 and Col. 4, Lines 1-18).

It would have been obvious to the one ordinary skill in the art in the time of invention to use approach as shown by Shimizu in the Sasaki et al., Arsenault et al., Hamai and Richards et al. apparatus to apply in downstream driver a voltage to LC cell in accordance with input video signal after receiving masking signal from upstream driver IC in order to suppress a disturbance of image on the panel (See Col. 3, Lines 20-21 in Taguchi et al. reference).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al., Arsenault et al., Hamai and Richards et al. as aforementioned in claim 1 in view of Babcock et al. (US Patent No. 5,623,519).

Sasaki et al., Arsenault et al., Hamai and Richards et al. do not teach about receiving video signal consisting of serial data, and wherein video signal is synchronized based on a synchronization pattern included in the serial data.

Babcock et al. shows how to synchronize serial stream based on a synchronization pattern included in the serial data (See Fig. 1, items 410, 430, in description See Col.1, Lines 48-67 and Col.7, Lines 42-54).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Babcock et al. approach in Sasaki et al., Arsenault et al., Hamai and Richards et al. apparatus in order to reduce size and increase reliability of the LCD display device.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al., Arsenault et al., Hamai and Richards et al. as aforementioned in claim 6 in view of Komarek et al. (US Patent No. 5,825,777).

Sasaki et al., Arsenault et al., Hamai and Richard et al. do not show a dummy circuit for substantially matching a video phase and a clock phase.

Komarek et al. teaches a dummy circuit matching operational characteristics modulating circuits (See Col. 10, Lines 7-18).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement dummy circuit as shown by Komarek et al. in Sasaki et al., Arsenault et al., Hamai and Richrds et al. apparatus in order to reduce size and increase reliability of the LCD display device.

5. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arsenault et al. in view of Sasaki et al., Hamai and Richards et al.

Arsenault et al. teaches receiver for receiving a video signal from a host (See Fig. 2, item 36, in description See Col.5, Lines 42-67); a sequencer for, upon the receipt of a control signal from host, generating header information for packet data, generating header information, based on a table, generated by sequencer to form a digital packet (See Fig. 2, item 60, in description See Col.6, Lines 1-6), to generate a digital packet information including input video signal (See Fig. 2, items 58, 60, 72, 84, in description See Col. 6, Lines 1-10) an how to filter incoming data by bit mask (See Fig. 5, item 140, in description See Col. 7, Lines 23-34 and Col. 2, Lines 39-40).

Arsenault et al. does not teach LCD driver comprising a plurality of driver ICs and video transmission line passing through each of the driver ICs in series, wherein driver ICs are

cascade connected in series and output means for converting video signal received from receiver into a serial video signal.

Sasaki et al. teaches and a plurality of signal lines, each of the signal lines passing through each of the driver ICs in series, wherein driver ICs are cascade-connected in series using signal lines (See Fig. 3, items 1-3,10, in description See Col. 4, Lines 34-43).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. approach in Arsenault et al. apparatus and to output means for converting video signal received from receiver into a serial video signal in order to provide a liquid crystal display device capable of achieving a larger screen size or higher resolution, without unnecessarily increasing dimensions (See Col. 2, Lines 26-30 in the Sasaki et al. reference).

Sasaki et al. and Arsenault et al. do not show connections to a power feed line via a metal layer inside of each driver ICs.

Hamai teaches outside power pad being connected to inside metal layers (See Fig. 1, items 2, 6, Col. 1, Lines 17-35).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Hamai teaching into Sasaki et al. and Arsenault et al. system in order to reduce area of power supply lines inside of the chip (See Col. 1, Lines 60-65 in the Hamai reference).

Arsenault et al., Sasaki et al. and Hamai do not disclose transmitting a wait bit block to a succeeding driver IC in series.

Richards et al. teaches disclose transmitting a wait block (See Fig. 10, item 130, from Col. 20, Line 54 to Col. 21, Line 18).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Richards et al. teaching into Sasaki et al., Hamai and Arsenault et al. system in order improved control system (See Col. 4, Lines 6-9 in the Richards et al. reference).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. in view of Arsenault et al., Kubota et al. (US Patent No. 6,335,778 B1), Hamai and Richrds et al.

Sasaki et al. teaches a video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs and a video transmission line (See Figs. 2-3, items 1-3,10,23 in description See Col. 4, Lines 27-45), driver ICs in series via a serial interface wherein the video transmission line passes through each of the driver ICs in series, and the driver ICs are cascade connected in series by video transmission line (See Figs, 3-4, items 1-2, 10, DATA, CNT, in Description See Col. 4, Line 28-67).

Sasaki et al. does not show transmitting a digital packet signal including video signal and each driver IC selectively generating a mask signal to mask video data output from the driver IC.

Arsenault et al. teaches to generate a digital packet information including input video signal (See Fig. 2, items 58, 60, 72, 84, in description See Col. 6, Lines 1-10) an how to filter incoming data by bit mask (See Fig. 5, item 140, in description See Col. 7, Lines 23-34 and Col. 2, Lines 39-40).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. controller using Arsenault et al. approach to the driver controlled by serial data line and generate a digital packet signal including input video signal and each driver

IC includes a controller for generating a mask signal to mask video data output from the driver IC since digital packets and masking has been well known and inexpensive.

Sasaki et al. and Arsenault et al. do not teach transmitting a synchronization pattern during horizontal blanking period in order to synchronize video signal for driver ICs.

Kubota et al. teaches synchronization with clock signal during the horizontal blanking period (See Fig. 5, items CKS, TRF, in description Se Col. 9, Lines 39-46).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. and Arsenault et al. controller using Kubota et al. approach transmitting a synchronization pattern during horizontal blanking period in order to synchronize video signal for driver ICs in order to be less affected by non-uniform properties of elements and that consume much less power (See Col. 4, Lines 51-54 in the Kubota et al. reference).

Sasaki et al. and Arsenault et al., Kubota et al. do not show connections to a power feed line via a metal layer inside of each driver ICs.

Hamai teaches outside power pad being connected to inside metal layers (See Fig. 1, items 2, 6, Col. 1, Lines 17-35).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Hamai teaching into Sasaki et al. and Arsenault et al., Kubota et al. system in order to reduce area of power supply lines inside of the chip (See Col. 1, Lines 60-65 in the Hamai reference).

Arsenault et al., Sasaki et al., Kubota et al. and Hamai do not disclose transmitting a wait bit block to a succeeding driver IC in series.

Richards et al. teaches disclose transmitting a wait block (See Fig. 10, item 130, from Col. 20, Line 54 to Col. 21, Line 18).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Richards et al. teaching into Sasaki et al., Kubota et al., Hamai and Arsenault et al. system in order improved control system (See Col. 4, Lines 6-9 in the Richards et al. reference).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. in view of Arsenault et al., Jayavant et al. (US Patent No. 6,204,864 B1), Hamai and Richrds et al.

Sasaki et al. teaches a video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs that are cascade connected (See Figs. 2-3, items 1-3,10,23 in description See Col. 4, Lines 27-45), transmitting a video signal via a serial interface wherein the video transmission line passes through each of the driver ICs in series, applying to an LCD a voltage based on video signal that is received and that is to be processed by each of driver ICs (See Figs, 3-4, items 1-2, 10, DATA, CNT, in Description See Col. 4, Line 28-67).

Sasaki et al. does not show transmitting a digital packet signal including video signal and each driver IC selectively generating a mask signal to mask video data output from the driver IC.

Arsenault et al. teaches to generate a digital packet information including input video signal (See Fig. 2, items 58, 60, 72, 84, in description See Col. 6, Lines 1-10) an how to filter incoming data by bit mask (See Fig. 5, item 140, in description See Col. 7, Lines 23-34 and Col. 2, Lines 39-40).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. controller using Arsenault et al. approach to the driver controlled by serial data line and generate a digital packet signal including input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC since digital packets and masking has been well known and inexpensive.

Sasaki et al. and Arsenault et al. do not teach video signal is constituted by bit blocks having plurality of attributes and wherein driver ICs are controlled by using bit blocks.

Jayavant et al. teaches bit blocks transfer and the font attribute (See Figs. 4-5, items 41,48, in description See Col. 5, Lines 56-58).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Sasaki et al. and Arsenault et al. controller using Jayavant et al. et al. approach to video signal constituted by bit blocks having plurality of attributes and wherein driver ICs are controlled by using bit blocks in order to maximize memory bandwidth for screen refresh(See Col. 4, Lines 11-13 in the Jayavant et al. reference).

Sasaki et al. and Arsenault et al., Jayavant et al. do not show connections to a power feed line via a metal layer inside of each driver ICs.

Hamai teaches outside power pad being connected to inside metal layers (See Fig. 1, items 2, 6, Col. 1, Lines 17-35).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Hamai teaching into Sasaki et al. and Arsenault et al., Jayavant et al. system in order to reduce area of power supply lines inside of the chip (See Col. 1, Lines 60-65 in the Hamai reference).

Arsenault et al., Sasaki et al., Jayavant et al. and Hamai do not disclose transmitting a wait bit block to a succeeding driver IC in series.

Richards et al. teaches disclose transmitting a wait block (See Fig. 10, item 130, from Col. 20, Line 54 to Col. 21, Line 18).

It would have been obvious to the one ordinary skill in the art in the time of invention to implement Richards et al. teaching into Sasaki et al., Hamai, Jayavant et al. and Arsenault et al. system in order improved control system (See Col. 4, Lines 6-9 in the Richards et al. reference).

8. Applicant's arguments filed on 03-31-05 with respect to claim 1, 3, 6-7, 9-10, 12, 14 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

9. Claims 11, 13, 15-16 are allowed.

10. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Relative to claim 11, the major difference between the teaching of the prior art of record (Sasaki et al., Arsenault et al., Hamai and Richards et al.) and the instant invention is that

the said prior art **does not teach** output means provide header information used for synchronization during a horizontal blanking period.

Relative to claim 13, the major difference between the teaching of the prior art of record (Sasaki et al., Arsenault et al., Hamai, Kubota et al. and Richards et al.) and the instant invention is that the said prior art **does not teach** synchronization pattern is transmitted for at least at two cycles, and wherein, during the period in which video signal is transmitted, driver ICs conform to synchronization pattern.

Relative to claim 15, the major difference between the teaching of the prior art of record (Sasaki et al., Arsenault et al., Hamai and Richards et al., Jayavant et al.) and the instant invention is that the said prior art **does not teach** one of bit blocks includes a wait command for waiting for driver ICs, and wherein wait command is generated by each of driver ICs that processes video signal and transmitted to a downstream driver that is cascade-connected.

Relative to claim 16, the major difference between the teaching of the prior art of record (Sasaki et al., Arsenault et al., Kubota et al., Hamai and Richards et al., Jayavant et al.) and the instant invention is that the said prior art **does not teach** video signal is transmitted to LCD driver by using a packet, and wherein plurality of driver ICs are controlled by a protocol that employs the header of packet.

Relative to claim 17, the major difference between the teaching of the prior art of record (Sasaki et al., Arsenault et al., Hamai and Richards et al.,) and the instant invention is that the said prior art **does not teach** during reception of video data, each driver IC transmits the wait bit to said succeeding driver IC; and during reception of the wait bit, said succeeding driver IC does not process any video data and waits to receive video data from said each driver IC..

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
07.19.05

VIJAY SHANKAR
PRIMARY EXAMINER